Amendments to the Drawings:

The attached drawing sheet includes changes to Fig.1B. This sheet, which includes Fig. 1B replaces the original sheet including Fig.1B.

Attachment: Replacement Sheet

Appl. No. 10/817,421
Response to Office Action Mailed September 27, 2006

PATENT

REMARKS/ARGUMENTS

No claims have been amended, canceled or added by the instant response. Accordingly, claims 1-17 remain pending in the instant application

In the latest Office Action, the Examiner objected to the drawings for informalities. In particular, the Examiner objected to Figure 1B as being mislabeled. Accordingly, Applicants have amended Figure 1B as suggested by Examiner.

Turning now to address the rejection of the claims based upon the alleged prior art, embodiments of present invention relate to a disk drive controller and system for correcting multiple burst errors in data bytes. More particularly, embodiments in accordance with the present invention correct data bytes utilizing block level and codeword check bytes in a two level block structure.

Accordingly, independent claims 1 and 9 recite as follows:

> 1. A disk drive controller that corrects multiple burst errors in data bytes, the disk drive controller comprising:
> a first level decoder; and
> a second level decoder that uses block level check bytes to detect columns in a two-level block structure of data bytes containing burst errors,
> . . . the first level decoder uses codeword check bytes in the two-level block structure to correct all of the data bytes in the columns identified by the erasure pointers, and
> the first level decoder does not use any of the codeword check bytes for error location calculations. (Emphasis added)
> ***
> 9. A disk drive system that corrects multiple burst errors in data bytes, the disk drive system:
> . . . a disk drive controller chipset that includes first level and second level decoders,
> wherein the second level decoder uses block level check bytes to detect columns in a two-level block structure of data bytes that contains burst errors,
> . . . the first level decoder uses codeword check bytes in the two-level block structure to correct all of the data bytes in the columns identified by the erasure pointers. (Emphasis added)

Claims 1, 2, 4, 5, 7-11, and 13-16 stand rejected as anticipated under 35 U.S.C. §102 based upon U.S. Patent No. 5,751,733 to Glover ("the Glover Patent). These claim rejections are overcome as follows.

As a threshold matter, the Examiner is respectfully reminded that pending independent claims 1 and 9, from which all other claims depend, stand rejected as anticipated, and not merely obvious, in view of the Glover Patent:

> [t]he distinction between rejections based on 35 U.S.C. 102 and those based on 35 U.S.C. 103 should be kept in mind. Under the former, the claim is anticipated by the reference. No question of obviousness is present. In other words, for anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. (Emphasis added; MPEP 706.02)

Here, the Glover Patent fails to teach either explicitly or impliedly a first and second level decoder utilizing block level and codeword check bytes to correct multiple burst errors.

There is no mention of the use of block level and codeword check bytes within the Glover Patent. The Glover Patent does disclose a method of using two levels, namely a track and sector level, for burst error correction. In the Glover Patent, however, the sector level decoder processes entire codewords in order to detect unrecoverable data (See col. 21, lines 43-50). This type of error detection would require additional processing causing the system to run slower and consume more memory. Accordingly, the Glover Patent fails to teach all of the elements of the pending claims.

In view of the failure the Glover Patent to teach each and every element of pending claims 1 and 9 explicitly or even impliedly, it is respectfully asserted that these claims cannot be considered anticipated by the art relied upon by the Examiner. Continued maintenance of the anticipation claim rejections is improper, and these claim rejections should be withdrawn.

Based on the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,
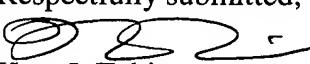
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